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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,974	01/15/2002	Eric C. Fox	5791	2770

7590 07/29/2003

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EXAMINER
TRAN, TAN N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/044,974	Applicant(s) FOX, ERIC C.	
	Examiner TAN N TRAN	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 06/19/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☒ Claim(s) *2-6,12-18 and 21-24* is/are allowed.

6)☒ Claim(s) *1 and 7-11* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/15/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings stand objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the CMOS circuitry process type well is formed to a greater depth than a depth of the first well as recited in claim 12, the CMOS process type well is formed to a greater concentration than the second concentration as recited in claim 13, an epi layer of the first conductivity type in a second concentration formed on the substrate, the second concentration being less than the first concentration; a first well of the first conductivity type in a third concentration as recited in claim 21, and an epi layer of the first conductivity type in a second concentration, the second concentration being less than the first concentration; a first well of a second conductivity type formed in the epi layer as recited in claim 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,7-11 stand rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe (6,448,104) (of record).

With regard to claims 1,10, Watanabe discloses a sensor formed in a substrate 100 of a first conductivity type in a first concentration p- comprising: CMOS circuitry to control the sensor; a first well 110 of the p^- type in a second concentration formed in the substrate 100, the second concentration being greater than the first concentration; and a photodiode region 130 of a n+ type formed completely within the first well 110; and CMOS image sensor serves as CMOS circuitry having the transistors 1 to 3 formed in the p well 110. Note lines 41-46, column5; and lines 1-8, column 3, figs. 10A-10C,12C of Watanabe. It is inherent that the CMOS circuitry includes at least one FET formed in a CMOS process type well of the p^- type because the conventional CMOS circuitry normally comprising the n-channel FET and p-channel FET.

With regard to claim 7, it is inherent that a gate electrode insulatively spaced over the first well 110 and disposed to control a transfer of charge between the photodiode region 130 and predetermined region 131 of the second conductivity type because the gate electrode controls the charges that move from the source region to the drain region. Note figs. 10A-10C of Watanabe.

With regard to claim 8, Watanabe discloses the predetermined region 131 of the second conductivity type is formed in the first well 110. Note fig. 10C of Watanabe.

With regard to claim 9, since Watanabe discloses the substrate 100 having a first concentration and having first intrinsic potential and the well 110 having second concentration

that is greater than the first concentration and a second intrinsic potential. It is inherent that the first and second intrinsic potentials induce a field between the substrate 100 and the first well 110 that repels photo generated charge from drifting from the substrate 100 into the first well because such structure of Watanabe is formed the same that of applicant, so the structure of Watanabe has the same functions as structure of applicant.

Applicant's claim 11 does not distinguish over Watanabe references regardless of the process used to form the CMOS process type well and the first well because only the final product is relevant, not the process of making such as "single processing step, the single processing step including one of ion implantation and dopant diffusion".

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases, as the above case law makes clear.

Allowable Subject Matter

3. Claims 2-6,12-18,21-24 are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as a pinning layer of the first conductivity type formed to a shallow depth in the photodiode region and electrically coupled to the substrate as recited in claim 2, the CMOS well is formed to a lesser depth than a depth of the first well as recited in claim 12, and the CMOS process type well is formed to a lesser concentration than the second concentration as recited in claim 13, a photodiode region of the second conductivity type formed in the second well as recited in claim 14, an epi layer of the first conductivity type in a second concentration formed on the substrate, the second concentration being less than the first concentration; a first well of the first conductivity type in a third concentration as recited in claim 21, an epi layer of the first conductivity type in a second concentration, the second concentration being less than the first concentration; a first well of a second conductivity type formed in the epi layer as recited in claim 22, a second well of the first conductivity type in the second concentration, wherein the predetermined region of the second conductivity type is formed in the second well as recited in claim 23.

Response to Arguments

4. Applicant's arguments filed 06/19/03 have been fully considered but they are not persuasive.

At page 11 of the remark, that "A request for approval of Drawing corrections is hereby attached to conform the drawings to the specification". However, the examiner has not received any drawing corrections as the amendment filed on 06/19/03 said.

It is argued, at pages 11,12 of the remarks, that "Watanabe does not disclose a sensor that includes both CMOS circuitry and photodiode region formed in a first well", "Figs. 10A, 10B, and 10C of Watanabe does not disclose both an n-channel FET and a p-channel FET", "Watanabe does not disclose any relationship between CMOS circuitry and the device depicted in FIGS. 10A, 10B and 10C" and "Watanabe does not disclose a sensor that includes both CMOS circuitry and photodiode region formed in a first well". However, lines 41-46, column5; and lines 1-8, column 3, figs. 10A-10C,12C of Watanabe does show a photodiode region 130 of a n+ type formed completely within the first well 110; and CMOS image sensor serves as CMOS circuitry having the transistors 1 to 3 formed in the p well 110. Thus, it is inherent that the CMOS circuitry formed in the first well 110 and the CMOS circuitry normally comprising the n-channel FET and p-channel FET. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., CMOS circuitry formed in a first well that including a photodiode region) are not recited in the rejected claims 1 and 10. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Election/Restrictions

5. This application contains claims 19,20 drawn to an invention nonelected with traverse in Paper No. 6. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Conclusion

6. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

July 2003

Minhloan Tran
Primary Examiner
Art Unit 2826